The Innovation

Laptops and tablets are wildly popular within different groups and demographics for being able to deliver specialized experiences to their users. Laptops have made significant strides in power, functionality and performance. Tablets, on the other hand, are currently the pinnacle of mobile technology. They are compact, light-weight and portable. However, their functionality as a computing device is still limited. Tablets are currently ideal to casually browse the Web to read news, participate in social media, play "lightweight" games, watch videos, etc. Tablets have also been seeing increasing use in music production, designing, financial trading and other fields.

Despite these advances in some niche area, tablets are often not suitable for Information Technology (IT) replacement which requires the capability of running compilers for programming, executing mathematical simulations, and/or heavy computing – tasks sought after by a larger segment of the population.

We propose a novel approach to tackle this problem, where we utilize Field Programmable Gate Array (FPGA) based portable hardware, which can be reconfigured to specific required applications, in order to accelerate compute intensive operations. This is particularly useful for operations with limited parallelism and significant control flow for which a Graphics Processing Unit (GPU) would be unsuitable. This device can be plugged into existing Tablets to act as an accelerator. FPGA based hardware has the added advantage of low power consumption, high performance, low cost compared to processors, with increased flexibility and dramatically reduced time to market resulting in decreased design and manufacturing time compared to Application Specific Integrated Circuit (ASIC) accelerator solutions.

Further, in order to protect against invasion of specific class of hardware Trojans through third party Intellectual Property (IP) cores, Dr. Sengupta's dual modular redundancy based security scheme during architectural synthesis will be integrated. This methodology will provide resiliency against hardware Trojan maliciously inserted by an adversary in a third party IP core. The goal of this algorithm will be to detect any such malicious Trojan in the system and signal an error. Although providing the layer of security against Trojan may add overhead, however we intend to optimize (in terms of latency and area) it through advanced evolutionary approaches. Thus coming up with a novel low cost Trojan security aware methodology at higher design abstraction level.

Additionally, in order to safeguard against threat such as IP core piracy, counterfeit, theft, false claim of ownership etc, Dr. Sengupta's multi-variable watermarking during architectural synthesis will be integrated. The novel watermarking technology devised at highest design abstraction layer will also provide protection against lower design levels. The watermarking technology incurs minimal design overhead, strongest security and high fault tolerance. It also will not degrade the actual design and functionality.

We plan also to leverage FPGA products that utilize non-volatile memories (NVMs) to replace SRAM blocks in order to further minimize (especially static) power. This is critical for battery-powered Tablets. Currently products exist that utilize FLASH memory, but we expect magnetic (i.e., STT-MRAM) and possibly other types of NVM-based FPGAs to be available in the future to improve endurance and speed deficiencies of FLASH.

Our proposed FPGA based reconfigurable platform provides a high speed, low power, area efficient, low cost, and reduced time to market solution. Furthermore, we will leverage the FPGA's reprogrammability to increase capability, reusability, and flexibility. For example, we envision a system that can compile MATLAB C/C++ codes using our proposed custom FPGA-based compiler. Furthermore we envision use of mathematical libraries that can accelerate compute intensive tasks using the FPGA. These FPGA designs can be swapped in and out depending on the app running on the Tablet. Such features are not current standards offered by other companies.

The proposed approach has great potential to positively impact society by improving quality, efficiency and reliability of computing power that rely on them. Furthermore, such technology and approaches will improve the competitiveness of Reconfigurable Computing (RC) solution providers and will lower the cost and entry barriers for entrepreneurs and new business startups based on FPGA-accelerated Tablet applications. We envision direct integration in Tablets and even Laptops as well as retrofit accelerators that can be attached via USB or Thunderbolt interface to existing products.

Market Size

As per Intersect360 research report believe the fundamental growth drivers of the High Performance Computing (HPC) market remain strong. They expect commercial and industrial spending to become an increasingly important part of the overall HPC market, with High Performance Technical Computing (HPTC) lagging and High Performance Business Computing (HPBC) in growth due to its large public-sector constituency and somewhat greater maturity. They expect commercial and industrial spending on HPC to remain relatively strong, potentially outgrowing overall economic growth.

Some of the key findings are:

- The total HPC market in 2013 was $30.5 billion, up 2.5% from 2012.

- The HPC revenue compound annual growth rate to be 4.6% from 2013 to 2018, reaching $38.1 billion at the end of the forecast period.

- HPTC contributed 69% of total HPC market revenues in 2013, with HPBC contributing the remaining 31%.

- Servers will lead the market in terms of absolute revenue growth, adding about $2.4 billion to the market by 2018.

- The growth rate leader in HPC market is the smallest but most-discussed segment of the market: cloud/utility computing is expected to grow at an 18.6% CAGR to $1.4 billion in 2018.

Historically, FPGAs have been slower, energy consumer and achieved less functionality than ASIC. However, this is less and less true since the last few years, where FPGAs become very close to ASICs in terms of performances. Thus, since 1985 and the first commercial FPGAs (Xilinx), the FPGAs market still growing to represent $6.4 billion today. It will reach $10 billion by 2020 according to Grand View Research forecasts.

Combining growths of HPC and FPGAs then, not only offer an interesting new paradigm (that we propose in this project), but opens a huge commercial market which can't be satisfied without novel products such the one we will develop in our project.

Vijay N.H.

VIVIDSPARKS IT SOLUTIONS PRIVATE LIMITED

Target Customers

Our target customers are computer professionals need a long lasting small form factor device with the power to do what a laptop, or even a workstation, is capable of with 24 hour+ lifetimes and/or fast recharging capability. Our proposed device is lightweight, portable, and inexpensive. It can even be charged with after market battery packs that are also small and inexpensive. This device can make a Tablet usable for programming (and compilation), simulations, and other heavy computing tasks when cloud connectivity is not available (e.g., on flights, in locations without reliable Internet connections as are found throughout South Asia, etc.). They can also eliminate the dependence on expensive international data network capabilities. The number of professionals traveling between the US, Europe and South Asia or China is increasing and these devices can considerably improve their capabilities while on flights.

Additionally, we see a large market in schools, colleges, universities, research centers that may include both government and private entities. Considering world's fast paced adoption of electronic devices, such as Tablets, and the increasing use of these devices to computer related applications, we expect the demand on the usage of tablet devices to grow substantially.

Marketing Plan

We propose a three-phase commercialization plan. Initially, as we are creating our hardware IP cores, we will be releasing the corresponding source codes to the open source hardware community (e.g. opencores. org), in order to raise awareness of our proposed approach and obtain valuable feedback from early adopters. We will also continue to publish our work in international journals and conferences in order to receive a similar level of peer review and recognition from the academic and industrial communities, and raise product awareness through social media networking. We will demonstrate our system at conferences, symposia, and trade shows to get recognition for the product. Next, as we develop our initial hardware boards, we will provide free evaluation versions to service providers, academic institutions, and R&D centers. Assuming this initial approach gains traction, our third phase is to market both our IP cores (in terms of customized designs, platform support) and hardware boards to companies who might be interested in adopting our technology. Once we have companies who are interested to adapt our technology, we then license our IP cores. We also plan to sell our Printed Circuit Board (PCB) as standalone accelerator to our potential customers. In next section, we plan to have business models for our IP cores and PCB.

Revenue Model

From the above strategies we plan to come-up following 3 main revenue streams:

- Accelerator Integrated with Dr. Anirban Senguta's technologies
- IP core Integrated with Dr. Anirban Senguta's technologies
- Technology Know-how consultation

In order to drive these streams, we will use following steps:

- We will engage University professors who helps sell to our product in return for commission. However he may never actually take ownership of the product (or even handle it). They simply get rewarded for referring customers to a retailer when they make a sale.
- We will appoint distributors who helps sell to our product in return for commission.
- We will sell our product to our target consumers at a low price who look for high end computing.
- We will sell our working prototype to FPGA board vendors, Computer Automation Design (CAD) tool vendors in semiconductor business and mother board manufactures in semiconductor companies who in turn sell to their customers.
- We will consult to companies for technical know-how for their products
- Using our contacts we will directly sell our products to our potential customers. With this model we will have better control over price, distribution channel and will help to address customer issues. More importantly, this model help us to gain confidence of customers.

Potential Funding Sources

In order to raise funds for the project we will apply proposals to various Indian and Foreign funding agencies such as DST, DRDO, ARDB, GITA, SERB, Leverhulme Trust, NSF, etc. Usually these funding agencies grant maximum of INR 50,00,000 for 3 years. In the Financials section we have considered operating expenses using these grant guidelines except for Marketing; we think funding component for equipments as per the funding agencies guidelines might be adjusted to marketing for the project, by assuming IIT-Indore have equipments to carry-out the projects.

Financials

Pessimistic Assumptions

Sales

	Per Month (Year 3)	Per Month (Year 4)	Per Month (Year 5)
Accelerator integrated with Dr. Sengupta's Technologies	5 Customers	10 Customers	15 Customers
IP Core integrated with Dr. Sengupta's Technologies	100 Volumes	150 Volumes	200 Volumes
Technology Know-how Cosultation	5 Customers	10 Customers	15 Customers

$ 1 = INR 68.

Pricing

	Year 3 (in $)	Year 4 (in $)	Year 5 (in $)
Accelerator integrated with Dr. Sengupta's Technologies	800/Unit	1000/Unit	1200/Unit
IP Core integrated with Dr. Sengupta's Technologies	25/Unit	50/Unit	75/Unit
Technology Know-how Cosultation	100/hr @90hr/year	150/hr @90hr/year	200/hr @90hr/year

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VIVIDSPARKS IT SOLUTIONS PRIVATE LIMITED

Net Sales	Year 1 (in $)	Year 2 (in $)	Year 3 (in $)	Year 4 (in $)	Year 5 (in $)
Accelerator integrated with Dr. Sengupta's Technologies			48,000	120,000	216,000
IP Core integrated with Dr. Sengupta's Technologies			30,000	90,000	180,000
Technology Know-how Cosultation			54,000	162,000	324,000
Gross Sales			**132,000**	**372,000**	**720,000**
Cost of Goods sold					
Marketing			44,118		44,118
Operations and Product Developement					
One senior Research Staff	6,424	6,424	6,424	6,424	6,424
Consumabels	368	368	368	368	368
Contingencies	368	368	368	368	368
TA/DA	735	735	735	735	735
Overheads	1,471	1,471	1,471	1,471	1,471
Net Operating Expense	**9,366**	**9,366**	**53,484**	**9,366**	**53,484**
Net Income Before Tax	**(9,366)**	**(9,366)**	**78,516**	**362,634**	**666,516**
Tax @ 30%			23,555	108,790	199,955
Net Income After Tax	**(9366)**	**(9366)**	**54,961**	**253,844**	**466,561**

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Summary

	In $	In INR
Total Income after tax (Year 1 -Year 5)	756,634	5,14,51,112
Total Investment Sought for initial 3 years (Year 1 - Year 3)	73,216	49,78,688
Total Investment Sought for remaining 2 years (Year 4 - Year 5)	62,850	42,73,00
Total Investment Sought for 5 years (Year 1 - Year 5)	136,066	92,52,488

VividSparks proposes to share 35% of the income to IIT-Indore. However, it is negotiable.